REMARKS

Reconsideration of the above-identified application, as amended, is respectfully requested.

In the Office Action of September 30, 2004, the Examiner first objected to the drawing Figure 2 as not being in compliance with 37 C.F.R. §1.84(p)(4) as a reference numeral "30" is referenced to two elements in Figure 1 and 2. To address this objection, applicants' hereby submit a drawing Replacement Sheet comprising amended Figure 2 showing the novel error correcting system architecture according to a second embodiment of the invention as element 29 instead 30 which represents the clock generate circuit element in Figures 1-3. Consequently, an instance in the specification on page 7 has been changed to set forth the novel error correcting system architecture according to a second embodiment as an element number 29 in view of the drawing amendment. The Examiner is respectfully requested to remove the objection to drawing figures in view of this amendment. Applicants' further take this opportunity to correct an informality with respect to Figures 1 and 2 where an element 28 is recited for two different elements, a reset signal and as a monitor circuit in Figure 1. The drawing Figures 1 and 2 are additionally proposed to be amended to correct the informality by indicating the reset signal as a signal 27. Consequently, instances in the specification on pages 6-7 have been changed to set forth the reset signal as an element number 27 in view of the drawing amendments.

Further in the Office Action of September 30, 2004, the Examiner further objected to the specification as allegedly comprising a number of minor informalities on pages 4, 5, 6 and 8. Each of these has been corrected in amendments to the specification

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IN THE DRAWINGS:

Please enter substitute drawing sheet 1 of 2 provided herewith, comprising Figures 1 and 2 that have been modified as indicated to correct informalities with respect to element numbers 28 and 30.

provided herein. For example, in the paragraph bridging pages 11 and 12 the specification is being amended to set forth that the output of the comparator circuit 70 will generate signals 80 as shown in Figure 3. The Examiner is respectfully requested to remove the objection to the specification in view of these amendments.

Further in the Office Action of September 30, 2004, the Examiner rejected Claims 1, 2, 5, 11, 12 14 and 18 under 35 U.S.C. §103(a), as being allegedly unpatentable over Sasaki et al. (U.S. Patent Publication No. 2002/0114224 A1) (hereinafter "Sasaki") in view of Naffziger et al. (U.S. Patent No. 6,509,788 B2) (hereinafter "Naffziger") and further in view of Fukazawa (U.S. Patent No. 6,655,588 B2) (hereinafter "Fukazawa"). Further in the Office Action, the Examiner rejected Claim 3 as allegedly unpatentable over Sasaki, Naffziger and Fukazawa, as applied to Claim 1, and further in view of Li et al. (U.S. Patent No. 5,477,181) (hereinafter "Li") and, further rejected Claims 4 and 13 as allegedly unpatentable over Sasaki, Naffziger and Fukazawa, as applied to Claim 2, and further in view of Ornes et al. (U.S. Patent No. 6,748,567 B1) (hereinafter "Ornes"). Further in the Office Action, the Examiner rejected Claims 6-8, 15 and 16 as allegedly unpatentable over Sasaki, Naffziger and Fukazawa, as applied to Claim 2, and further in view of Lambrecht et al. (U.S. Patent No. 6,775,809 B1) (hereinafter "Lambrecht") and, further rejected Claim 9 as allegedly unpatentable over Sasaki, Naffziger, Fukazawa and Lambrecht, as applied to Claim 6, and further in view of Collier (U.S. Patent Publication No. 2002/0107897 A1) (hereinafter "Collier"). Further in the Office Action of September 30, 2004, the Examiner rejected Claims 10 and 17 under 35 U.S.C. §103(a), as being allegedly unpatentable over Sasaki, Naffziger and Fukazawa, as applied to Claim 5, and further in view of Tada et al. (U.S. Patent Publication No. 2001/0047319 A1) (hereinafter "Tada").

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Further in the Office Action of September 30, 2004, the Examiner objected to minor informalities in Claims 4 and 5 that are addressed in amendments to these claims provided herein. The Examiner is respectfully requested to remove the objection to Claims 4 and 5 in view of these amendments.

With respect to the rejection of Claims 1, 2, 5, 11, 12 14 and 18 under 35 U.S.C. §103(a), as being allegedly unpatentable over Sasaki and Naffziger in view of Fukazawa, applicants respectfully disagree in view of remarks and clarifying amendments herein.

The present invention as set forth in amended Claims 1 and 11 is directed to a system and method for dynamically optimizing a clock speed of a clock signal used for timing of data signal transmissions and receptions within an integrated circuit (IC) device. The system comprises: a transmitter means for successively transmitting data signals for receipt by a receiver device within said IC; and, a clock generator circuit for providing the clock timing signal used for timing the data signal transmission and reception within said IC. The Claims 1 and 11 have been further amended to set forth that each data signal transmission is transmitted at a different clock speed. A real time monitoring circuit is included having means for receiving successive data signal transmissions generated at different clock speeds and detecting when a data signal transmission fail point is achieved at a particular clock speed. A means is provided for adjusting the clock timing signal in real time according to a maximum speed allowed for the IC that avoids the data transmission fail point during real time operation. The invention thus provides for optimum timing of the source and receive logic since the clock frequency will be automatically adjusted to compensate for manufacturing

process conditions and operating parameters during operation (See page 4, lines 16-18 of the present specification).

Support for the claim amendment setting forth that each data signal transmission is successively transmitted at a different clock speed and support for the claim amendment characterizing the receiving means as receiving successive data signal transmissions generated at different clock speeds is found in the specification, for example, at page 3 lines 4 through 10, and at page 8 lines 11 through 19. Care has been taken to ensure that no new matter is being entered.

Respectfully, neither the Sasaki, Naffziger nor Fukazawa whether taken alone or in combination, teach the system and method for dynamically optimizing a clock speed in order to maximize data transmission speeds beyond a data transmission fail point caused by the real-time operating conditions of the transmission path in the integrated circuit.

Respectfully, the primary reference to Sasaki does not teach this. The Examiner has relied on Sasaki only to the extent that it deals with data transmission between a path comprising flip-flop elements in an IC. However, the Examiner is incorrect in stating that Sasaki provides "dynamically altering a clock speed" and has mischaracterized the Sasaki teaching as it is directed to a non-real time (i.e., off-line) design process that utilizes flip-flop transmission fan out delays as a parameter in designing circuits including these flip-flop elements so they may meet a desired machine cycle speed. As part of the off-line process, Sasaki teaches a design technique for providing physical adjustments that can be implemented for tailoring a speed of clock signals governing the timing of the flip-flop devices in a group of interconnected flip-flop devices. Thus, for example, as described on page 2, paragraph [0015] and page 3 paragraphs [0029] to [0032] of Sasaki, the Sasaki system is a design system

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whose innovation is determining how to design clock signal lines, for example, in order to achieve an increase or decrease in a clock timing for a particular circuit area or group of interconnected flip-flop elements. In Sasaki, thus, the design output would indicate at what distance to the flip-flop should the wire length be adjusted for receiving clock signals from the clock pin, providing so-called, "detour wiring", or at what capacitance should the clock input pin be designed, to increase a clock delay. Further, a design output in Sasaki would indicate at what point in an amplifier stage of a clock circuit to tap the clock signal from in order to decrease a clock delay (increase speed). Thus, Sasaki specifically teaches an off-line process for optimizing a circuit design for ensuring circuits including interconnected flip-flop elements perform according to a desired synchronous timing scheme (time equivalent to a machine cycle). Sasaki is thus not relevant as it only pertains to a design process for guiding a designer in making physical circuit design choices, i.e., Sasaki does not teach dynamic optimization of clock timing signals during real-time operation as required by Claims 1 and 11, as now amended.

The present invention as amended in Claims 1 and 11, teaches a system and method for providing real time clock speed adjustment so as to optimize data transmission through transmitter and receiver circuit elements utilizing successively transmitted data signals at different clock speeds. As a result of this data transmission stimulus, a real-time adjusting of the clock timing speed is performed that is used to maximize the data signal transmission and reception speed within the IC to a point short of a transmission failure. In one aspect, a continuous monitoring process and clock speed adjusting process is performed while the chip is in real time operation. It does this according to three embodiments set forth

in respective claims 4, 5 and 6 relating to embodiments depicted in Figures 1,2 and 3, respectively, of the present application.

The Naffziger reference is of no help in this regard. Naffziger teaches provision of a system for generating and altering clock signal frequency in real-time operating circuits, however, only for the purpose of optimizing power distribution/consumption in those circuits. The present invention is directed to optimizing clock signal speeds used for the transmission and receipt of data within an integrated circuit according to embodiments of Figures 1-3 (Claims 4-6).

The Fukazawa reference is further of no help in this regard as it does not teach data transmission between transmitter and receiver elements within an IC card- but rather teaches a manner for utilizing a parity bit for testing the content of data sent between two physically separated IC card (an IC card and IC card reader/writer) that are in communication. There is no clock signal timing optimization being performed in Fukazawa as in the present invention. When there is an error in a transmission between the two devices, Fukazawa only teaches requesting a retransmission from the transmitting side coupled with changing a voltage level of a signal line between the two devices for a predetermined time period, in order to facilitate a next data transmission request. Thus Fukazawa is not even remotely concerned with optimizing clock signal speeds used for the transmission and receipt of data within an integrated circuit according to embodiments of Figures 1-3 (Claims 4-6).

Thus, in traversing the Examiner's application of the Sasaki, Naffziger and Fukazawa applicants respectfully submit that the requisite motivation to combine the references to achieve the invention is not provided. That is, without the benefit of hindsight, a skilled artisan would not be motivated to combine the disparate and unrelated teachings of the

Sasaki, Naffziger and Fukazawa references. Sasaki is directed to a circuit design process that will enable the physical feeding of a clock signal circuits to interconnect flip-flop devices fan-out stages; Naffziger teaches real-time adjustment of a clock signal only for the optimization of power consumption in an IC; and, Fukazawa is unrelated as no clock timing signal optimization is being performed; Fukazawa only suggests the generating of data retransmission requests between two separated IC devices upon detection of a parity bit error in an original data transmission.

Respectfully, applicants do not see how this combination would teach the present invention, and the Examiner is respectfully requested to withdraw the rejections of Claims 1 and 11 under 35 U.S.C. §103(a). Accordingly, the Examiner is respectfully requested to withdraw the rejection of all claims dependent upon amended independent Claims 1 and 11.

With regard to the different embodiments for optimizing clock signal speeds used for the transmission and receipt of data within an integrated circuit according to embodiments of Figures 1-3 (Claims 4-6), applicants hereby have amended Claims 4 and 13 to clarify the provision of an error correction code signal generating circuit for generating error correction code signals according to each data signal transmission, wherein the monitoring circuit comprises an error correction code signal check circuit. With respect to the rejection of Claims 4 and 13 applicants respectfully submit the following:

Ornes, cited in the rejection of Claim 4, is not relevant in that it is directed to way of permitting clock recovery when errors are detected in ECC transmissions in communications lines. Ornes further only teaches checking the integrity of the ECC code itself to determine errors in the ECC codes transmissions themselves (see Ornes summary at

col. 2, lines 52-67). It is not related to optimizing of clock timing signals to ensure maximum

data signal transmission/receipt speeds within an IC circuit. At best, Ornes teaches the

repairing of a detected ECC error (see step 920, Figure 9 of Ornes) which is completely

unrelated to the present invention set forth in Claims 4 and 13.

Similarly, with respect to the rejection of Claims 6-8, 15-16, Applicants

respectfully traverse. Claims 6 and 15 are first being amended to clarify that a random data

generating circuit is provided for generating unique random data signals for <u>transmission</u>

<u>throughout a data path of a circuit within</u> the IC device, the circuit for processing said random

data signals. The cited Lambrecht reference in combination with the Sasaki, Naffziger and

Fukazawa references do not teach the present invention as set forth in these claims for the

reason that Lambrecht is only directed to determining performance characteristics of an IC

device and a transmission media enabling communication between two physically separate

devices (first and second IC devices over a transmission medium 108 as shown in Figure 10

and described at col. 10, lines 36-39). Lambrecht further does not teach not suggest dynamic

optimization of the clock signal to maximize speed of data transmissions/receptions short of a

stat transmission fail point within an IC during real-time operation. Lambreacht further does

not teach generating unique random data signals for <u>transmission throughout a data path of a</u>

<u>circuit within</u> the IC device – it is only concerned with checking the performance

characteristics of a transmission media –i.e., checking for presence of intersymbol

interference (ISI) e.g., that may be due to signal reflections or electromagnetic couplings. In

fact, Lambrecht is directed to determining worst case performance characteristics, e.g., worst

case timing margins or voltage margins (see Lambreacht at col. 2, lines 44-49, for example).

Thus, Lambrecht actually teaches away from the present invention as it teaches determining a

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worst case performance scenario- it does not provide a teaching of how to maximize system

data transmission performance by optimizing governing clock timing signals right before the

point of data transmission failure during real time operations.

Applicants further take this opportunity to correct a minor informality in Claim

12 in accordance with the amendments to Claim 11 provided herein.

In view of the foregoing remarks herein, it is respectfully submitted that this

application is in condition for allowance. Accordingly, it is respectfully requested that this

application be allowed and a Notice of Allowance be issued. If the Examiner believes that a

telephone conference with the Applicants' attorneys would be advantageous to the disposition

of this case, the Examiner is requested to telephone the undersigned, Applicants' attorney, at

the following telephone number: (516) 742-4343.

Respectfully submitted,

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